REMARKS

Pending Claims

Previously pending claims 21-35 as correctly renumbered by the Examiner have been cancelled to expedite prosecution of the application. Applicant submits new claims 36-41 for consideration with claims 36, 38, and 40 being independent.

Rejection: Non-Statutory Double Patenting

The Examiner rejected the previously pending claims under the non-statutory doctrine of double patenting. While Applicants have cancelled the previously pending claims, Applicants have nevertheless included a terminal disclaimer with this response to expedite prosecution of the application.

Rejection of Cancelled Claim 21

While Applicants have cancelled claims 21 -35 to expedite prosecution of the application, Applicants would like to express disagreement with the Examiner's position regarding the previously pending claims both in anticipation that the Examiner may consider similarly rejecting new claims 36-41 and to prevent the conclusion that the Applicants conceded that the previously pending claims were either anticipated or obvious in view of Wazlowski and/or Trimberger.

Cancelled claim 21 recited "a plurality of microengines that support multiple hardware threads". The Examiner rejected claim 21 as anticipated by Wazlowski (PRISM-II Compiler and Architecture), identifying the array of FPGA (Field Programmable Gate Arrays) as providing the recited microengines. Applicants disagree, however, that the FPGAs are multi-threaded microengines. As understood by the Applicants, Wazlowski describes a system that reconfigures the logical networks of the FPGAs to optimize processor architecture based on a given program. For example, based on a particular program that frequently performs operation "x" and "y", the configuration compiler of Wazlowski may determine how to configure a first one of the

FPGAs to perform "x" and another FPGA to perform "y". When these operations are encountered during execution of a software image of the program by the AM29050-33 processor, the processor uses the FPGAs to quickly perform the operation in FPGA hardware. In essence, the system of Wazlowski effectively extends the hardware executable instruction set provided by the processor to include "special" instructions tailored for a particular program. Attorney for the Applicants readily admit that Wazlowski sounds like a really cool idea! However, Applicants strongly disagree that implementing a given operation in a FPGA is the same thing as one (or multiple) thread(s) of execution. That is, hardware (whether dynamically configured like a FPGA or dedicated circuitry) to perform a particular operation (e.g., ADD a, b) is not the same thing as hardware that provides multiple threads of program execution.

Nor does Trimberger et al. ("A Time-Multiplexed FPGA") describe multiple threads of execution. Trimberger describes a system that reconfigures a FPGA to perform different operations at different times. For example, the FPGA may be configured to perform ADD a+b at one time and SUB a-b at another. Again, however, an operation provided by a FPGA does not constitute thread. Nor do multiple operations provided by a FPGA at different times constitute multiple threads.

Conclusion

Applicants respectfully request allowance of the pending claims.

The Examiner is encouraged to call the undersigned at 978-553-2060 to discuss any informalities or substantive issues.

If any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing attorney docket number: 10559-075002.

Respectfully submitted,

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